

REMARKS

Applicant would like to thank the Examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office action, and amended as necessary to more clearly and particularly describe the subject matter which applicant regards as the invention.

Claims 4-9 and 13-20 have been indicated as containing allowable subject matter and, therefore, will not be discussed hereinafter.

Claims 1-3 and 10-12 stand rejected as being unpatentable over US 6,204,622 to Tsuruta in view of JP 08-084490 to Yoshizawa. For the following reasons, the Examiner's rejections are traversed.

The present invention is directed toward solving problems that are encountered in conventional controllers. More particularly, and as noted in the Background section of the present application, "[i]n the conventional controllers, as shown in Fig. 12, after the position command has become zero, the positioning response is delayed for an amount corresponding to a residual quantity of the remaining integrated value in the speed integrator 32 (Fig. 10, item 32)." The inventions defined in claims 1 and 10 use a speed control delay compensation low-pass filter 133 in order to solve this problem.

In this regard, each of claims 1 and 10 define that the speed control unit includes "a delay compensation low-pass filter in the speed control unit has a transfer function corresponding to a delay of a speed control system". In the application it is noted that "with the use of the delay compensation low-pass filter in the speed control unit as proposed in the present invention, the difference between

the speed indicated by the speed command with a delay corresponding to the delay of the speed control system and the actually delayed fed-back speed can be rendered nearly zero. This makes the residual quantity in the speed integrator almost zero. Thus the positioning time is shortened.” Page 6, line 19, to page 7, line 1. These features of the invention, while believed to be inherently included in claims 1 and 10, are specifically defined in new claims 21 and 22.

Tsuruta and Yoshizawa do not teach or suggest such speed control delay compensation low-pass filter as required by the invention defined in claims 1 and 10.

According to the configuration of the speed control unit 13 disclosed in Tsuruta, a difference between a speed command V_{ref} and an output FV_{fb} from the speed feedback filter 131 is input into the integrator 133.

On the other hand, in the present invention, a speed command is inputted into the speed control delay compensation low-pass filter 133, as shown in Fig. 1. Then, a delay speed command is outputted from the speed control delay compensation low-pass filter 133. A deviated difference between the delay speed command and a fed-back speed is integrated by the speed integrator 132. Therefore, Tsuruta does not disclose the speed control delay compensation low-pass filter 133. It is noted that the Examiner has acknowledged this deficiency of Tsuruta, and has cited Yoshizawa as teaching this feature of the present invention.

In the Office action the Examiner has cited Yoshizawa as disclosing "a speed control method for a motor, which includes a delay compensation low pass filter/compensation circuit (Fig. 1 item1; refer to the constitution) in the speed control section having a transfer function corresponding to a speed control system. It should be noted that the compensation unit of Yoshizawa can be implemented

within a singular speed control unit for controlling the motor.” From this interpretation of Yoshizawa, the Examiner has concluded that “It would have been obvious to one of ordinary skill in the art at the time of invention to use Yoshizawa’s compensation circuit with the invention of Tsuruta. The advantage of combining the two inventions would provide a system that can speed productivity of a system while avoiding degradation quality by employing a compensation type circuit.”

However, it is noted that the speed compensation circuit 1 disclosed in Yoshizawa is different from that of the present invention in respect of functions. In the speed compensation circuit 1, the achieved speed follows up a reference speed even when the response of a speed control system cannot be ensured sufficiently.

As shown in expression (11), a transfer function $G_{CMP}(S)$ of the speed compensation circuit 1 is constituted by quadratic differential.

$$G_{CMP}(S) = (T_1 \cdot T_2 \cdot S^2) / (1 + T_1 S) \text{ ----- (11)}$$

With this transfer function, conventional speed response characteristics shown in Fig. 4 can be improved into speed response characteristics shown in Fig. 2. For the Examiner's reference, translations of Fig. 2 and Fig. 4 are attached hereto.

Thus, the speed compensation circuit 1 of Yoshizawa is intended to improve the speed response characteristics, and does not improve positioning response delay based on a residual quantity of the remaining integrated value in the speed integrator. Therefore, even with the use of the speed compensation circuit 1 of Yoshizawa having a transfer function constituted by quadratic differential, it is impossible to reduce a residual quantity of the remaining integrated value in the speed integrator almost to zero, and accordingly to shorten the positioning time,

which is the purpose of the instant aspect of the present invention.

As described above, the speed compensation circuit of Yoshizawa is quite different from the speed control delay compensation low-pass filter of the present invention. Therefore, even if Tsuruta and Yoshizawa were combined, the present invention would not result.

Thus, reconsideration and withdrawal of the rejections of claims 1 and 10 is requested. Insofar as claims 2-3 and 11-12 depend from claims 1 and 10, respectively, reconsideration and withdrawal of the rejections of these claims is also requested.

In light of the foregoing, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 18-0160, our Order No. NIS-16060.

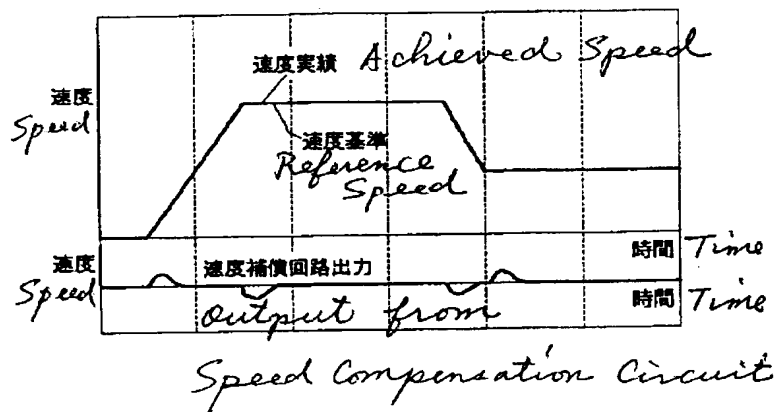
Respectfully submitted,

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【図2】 Fig. 2



【図4】 Fig. 4

